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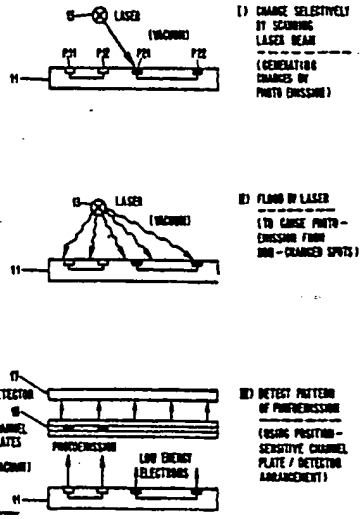
(54) Testing method for integrated circuit packaging boards using a laser in vacuum.

(57) For testing the integrity of conducting lines on or in a substrate , the following steps are executed: (I) Selected pads (P21) are irradiated by a focused laser beam so that they are positively charged due to photoemission of electrons. The charges propagate through existing conductors so that all selected pads (P21) and all pads connected to them (P22) assume a specific voltage. (II) The whole surface is irradiated by a flooding laser beam. Photoemission of electrons will now occur from those pads which were not charged previously (P11, P12). (III) The photoelectrons emitted in step II are detected by a channel plate arrangement and a position-sensitive detector thus revealing the spatial distribution of uncharged pads. This method is performed in vacuum and allows completely contactless testing of circuitry to detect line interruptions as well as shortcuts between separate lines. It is suited for surface lines, buried lines, and in particular also for via connections.

FIG.1 PRINCIPLE



EP 0 264 481 A1

TESTING METHOD FOR INTEGRATED CIRCUIT PACKAGING BOARDS USING A LASER IN VACUUM

FIELD OF INVENTION

Present invention is concerned with the testing of electrical connections in circuit substrates, and in particular with the testing of interconnection lines and via connections in boards for packaging integrated circuit chips. It is generally suited for testing conducting lines and via connections in substrates.

BACKGROUND

The testing of integrated circuits and of their interconnections in packaging is an important task in the manufacturing of electronic and data processing equipment. It is particularly important that the testing methods are fast and do not require much preparatory operations for their execution.

In principle, testing can be done by applying power and data signals to, and extracting resulting data signals and electrical conditions from, circuit y through the regular connection pins, or through mechanical contact probes. Such testing is, however, slow and not very effective because of the limited number of connections which can be made. It is therefore not well suited for highly integrated circuits and dense packaging which are used today.

Therefore, some methods of contactless testing have been recently suggested using either electron beam or laser technology. E-beam testing was described in an article by E.Menzel et al.: "Fundamentals of Electron Beam Testing of Integrated Circuits", published in Scanning, Vol.5 (1983), pp.103-122. The E-beam is used as a contactless probe, either in a passive or active mode. However, the utilization of electron beams for testing has certain disadvantages and limitations. Scanning or flooding a substrate by an E-beam leads also to the charging of the substrate because the incident electrons have energies much larger than the work function of the substrate, i.e. they produce secondary electrons. This strongly influences the voltage contrast between different points on a substrate and hinders the measurements. Furthermore, reflected high energy electrons strongly complicate simultaneous measurement for many different points using position-sensitive detectors because these high energy electrons must be separated from the lower energy electrons which carry the required information.

More recently, the use of a laser beam for integrated circuit testing has been suggested. The photons of a laser beam can excite electron emission from the target, and the laser beam can thus be used for contactless testing of electronic circuitry.

European Patent Application EP-A-..... (86103212.6) entitled "Noncontact Testing of Integrated Circuits" discloses a technique of directing a laser beam in a scanning motion to lines of test points so that photoelectrons are generated in dependance of the operating conditions of those test points; the generated electrons are then directed to a two-dimensional array electron detector so that an analysis can be made.

In European Patent Application EP-A-..... (86110460.2) a testing procedure is described in which laser light is directed to the entire surface of a circuit chip, and in which that laser light causes generation of photoelectrons in dependance of the voltage present at each point. The electrons generated are directed either to a luminiscent target whose image is then evaluated, or the electrons are directed to channel plates and further to a luminiscent target and an optical processing system.

In both systems disclosed in the two above-mentioned European patent applications, power and test data signals have to be applied to the tested circuits through normal pins and chip connections, to bring them into an operating status that is to be detected in the testing procedure. This is a limitation of the testing possibilities.

OBJECTS OF THE INVENTION

It is a primary object of present invention to provide a testing method which is completely contactless and thus does not require the establishment of connections for the application of power and test data to the circuits to be tested.

It is a further object of this invention to devise a testing method which is particularly suited for testing the conducting lines in packaging boards for integrated circuitry.

Another object of the invention is to provide a testing procedure which does not require application of electron beams and which thus can achieve high voltage contrasts.

A further object is a testing method which enables simple, fast, and simultaneous testing of via connections through a substrate.

DISCLOSURE OF THE INVENTION

In the invented method for achieving these objects, a laser is first applied to predetermined pads of circuitry on a substrate to cause photoemission therefrom so that they are charged positively; this will bring these predetermined pads and all conducting lines and pads connected to each of them, to a particular voltage level. Thereafter, the laser beam is directed to the board surface a second time to excite photoemission from pads, whose intensity is now depending on the voltage previously established at each pad. The photoelectrons are directed to a channel plate arrangement for amplification, and the resulting pattern of intensities is evaluated to thus detect which pads are actually in electrical connection with the predetermind pads and which are not.

This method has the advantage that it can be used for surface lines, buried lines, as well as for via connections. It allows the simultaneous testing of several connections which is e.g. not possible with E-beam technology.

Embodiments of the invention will be described in the following with reference to the drawings.

LIST OF DRAWINGS

Fig.1 is a schematic representation of the sequential steps of the invented testing method for testing connections between pads on one side of a circuit board;

Fig.2 is a schematic representation of the sequential steps of the invented method for testing via connections;

Fig.3 shows the essential components and their interrelationship in a testing facility for executing the invented method;

Fig.4 illustrates the testing possibilities of the invention for different line structures and connections.

DETAILED DESCRIPTION

1) PRINCIPLE OF INVENTION

The testing procedure of present invention is of primary interest for packaging, i.e. for testing the circuits and conducting lines which are provided between pads on circuit boards. Such circuit boards are used for carrying and interconnecting individual chips which were tested already previously.

Fig.1 is a schematic representation of the new testing method. The three main steps of the method are represented in the three portions I, II, and III of the drawing. It should be noted that the testing is done in vacuum, to enable photoemission from a surface which is irradiated by a laser beam.

In the first step (I) the circuit board 11 containing the circuits or conductors to be tested is subjected to a laser beam from laser device 13 (ultraviolet laser). The laser beam can be directed to selected spots on the board 11 by a scanning mechanism, and it can be switched on and off. There are shown two pairs of pads P11/P12 and P21/P22, each pair being interconnected by a conductor which is to be tested. In this first step, one of the pads, e.g. P21, is subjected to the laser beam. Due to photoemission from the conducting material at this spot, pad 21 will be charged positively, but not the surrounding insulator surface of board 11. The reason for this good contrast is the fact that the photon energy for the laser irradiation is chosen such that it is large enough to excite photoelectrons from the metallic pads, but is too small to excite photoelectrons from the ceramic substrate. A grid should be provided for collecting the generated photoelectrons (as shown in section 2).

The charges collecting on the selected pad P21 will propagate through all portions of the electrical circuitry which are connected to P21, in this case through the conductor to pad P22. Thus, at the end of step (I), P21 and also P22 should be at a different potential than all other surface spots of the board, if the circuitry between P21 and P22 is intact. However, if there would be a discontinuity in the conductor between P21 and P22, P22 would not be at the higher potential; furthermore, if there would be a short circuit connection between P21 and P12, the charges would distribute to both pads P12 and P11 so that both would be at the higher potential which is also present on P21 and P22. The specific voltage level at the selected pads and pads connected to them will depend on the laser power used, the irradiation time, and the conductor material.

Therefore, by first selectively charging selected points of the circuitry to be tested, and then detecting on which non-irradiated spots the higher potential appears, defects in the circuitry or conductors can be determined.

Steps (II) and (III) are executed for the detecting operation which actually is a voltage-contrast measurement. In step (II), the whole surface of board 11 is flooded by a wide-spread laser beam from laser device 13. This will cause photoemission from all metallic points. But the electrons from the previously charged spots will have a lower kinetic energy than the electrons from uncharged spots.

These lower energy electrons will not be able to pass through a barrier to a detection arrangement. Thus, there will be no detectable photoemission from those metallic spots which are at a higher potential than the other metallic spots on the surface of board 11; in the case of intact circuitry, these spots would be pads P21 and P22 in the present example.

In step (III), the photoemission pattern from non-charged metallic surface areas is detected. An arrangement of channel plates 15 and a position-sensistive detector 17 are used for this purpose. Such channel plates 15 are a high-density array of electron multiplier plates and are well known. They produce a high gain in the photo-electron intensity. Position-sensitive detector 17 which may be a luminiscent phosphor plate or a semiconductor plate of which each spot can be charged separately reveals the spatial distribution of detected electrons which is an indication for the location of all uncharged metallic spots on the board's surface. This spatial information can be converted to a time-sequential data sequence and then e.g. be stored or directly processed in a computer for obtaining the test results. Of course, electrical grid means must be provided in the vacuum between the board 11 and the channel plates 15, to correctly collect the higher energy photoelectrons and to refuse the lower energy photoelectrons. These details will be explained in the following section 2.

Testing of Via Connections:

So far, the testing was only done on one side of the board. For testing via connections, i.e. conductors between pads on different surfaces of the board, the board would either have to be turned over after step (I) - if the induced charges sustain for a sufficient long time - or a flooding laser and the channel plate/detector arrangement would have to be provided on the other side of the board, as is shown in Fig.2. In the case of Fig.2, via connections are provided between pairs of pads P31/P32 ... P61/P62, respectively, which are located on opposite sides 11A and 11B of the board. Otherwise, procedure steps I, II, and III correspond to those described in connection with Fig.1.

There is of course also the possibility of testing all via connections in a board simultaneously. In this case, step (I) of the procedure would consist of flooding the whole surface area 11A with a laser beam to charge all via pads located on that side of the board. Then, for all intact vias the respective pads on the other surface 11B would be charged; for each interrupted via, the corresponding pad on the other surface 11B would have no charge. Steps (II) and (III) for simultaneous via testing are the same as for individual via testing: flooding of the whole other surface 11B by a laser beam, and detecting the photoemission pattern by the channel plate/detector arrangement.

2) EMBODIMENT OF A TESTING FACILITY USING THE INVENTION

Fig.3 illustrates a testing facility in which the invention is used. This facility includes a vacuum chamber 19 having a base plate 21. A support 23 is provided for holding circuit board (package substrate) 11. On the surface of board 11, electrical connection pads 25 are shown schematically. Circuits or conductors to be tested are not shown in this drawing.

Laser device 13 comprises a source 27 of ultraviolet laser light and a scanner/flooder arrangement 29. Scanner/flooder 29 is a suitable means for focussing and deflecting the laser beam emitted from source 27 to selected points on board 11, or for providing a wide-angle laser beam covering the whole surface of board 11. The scanner/flooder may be a commercial system as used in purely optical laser scanning microscopes, based on a rotating polygone mirror plus focusing/beam spreading objective. As such focusing and deflection means are well known they need not be described here in more detail.

A control unit 31 is provided for furnishing suitable control signals for laser source 27 (switching the beam on and off) and for scanner/flooder 29 (coordinate signals for selected points to be charged for testing, or control signal for providing a wide-angle laser beam). The basic data for any testing procedure are stored in a processor/storage 33, and are furnished to control unit 31.

Channel plates 15 are provided for receiving in true spatial relationship the photoelectrons emitted from the surface of board 11 in response to the flooding by a laser beam in step (II) of Fig.1. Two grids are provided for collecting photoelectrons from selected pads in step (I), and for achieving a good transfer of photoelectrons to the channel plate arrangement in step (II): An accelerating grid 35 which has an electrical potential (V_{ACC}) that attracts and thus accelerates the photoelectrons from board 11. A typical potential for this grid 35 would be 100 Volts. To refuse the lower energy photoelectrons and thus to enable voltage discrimination, a retarding grid 37 is provided which has a retarding potential (V_{RET}) to slow down the electrons which have passed grid 35. A typical potential for this grid 37 would be between -10 Volts and +10 Volts. A

voltage source 39 is provided for furnishing the potentials (V_{ACC}) and (V_{RET}) to the grids. It receives control signals for selecting the correct grid potentials from control unit 31.

The electrons furnished by channel plates 15, which represent the spatial distribution of potentials of metallic spots on the surface of board 11 propagate to position-sensitive detector 17. If this is a luminiscent layer, its image can be recorded by a TV camera. The scanning signals of this camera which are a sequential representation of the spatial illumination distribution on detector 17 can then be evaluated. If the detector is a chargeable semiconductor plate it can be read out directly by a commercial charge coupled device (CCD) camera which acts as a signal evaluator 41. This signal evaluator furnishes the test result data sequentially to processor/storage unit 33 from where they can be extracted for a final evaluation of the test, or for producing a printout of the test results for the respective board.

3) CIRCUIT/CONDUCTOR CONFIGURATIONS WHICH CAN BE TESTED

Fig.4 illustrates the different basic testing possibilities which are available when using the testing method of present invention.

In Fig.4A there are shown a few simple connections A1, A2, A3, and A4 between pairs of pads. All of these connections are located at the surface of the board, as can be seen in the sectional side view. For testing, a laser beam is first selectively directed to the left pad of connection A1, A2, or A3 in method step I (each connection is separately tested). In the figure, this is indicated by an arrow with an "L". The detection in method step III is indicated by an arrow with a "D". For normal connection A1 the detection will show that the charges have propagated to the right pad (indicated by a "1"). For interrupted connection A2, the expected potential will not be detected at the right pad (indicated by a "0"). For normal connection A3 the result at the right pad is the same as for A1. However, a short circuit is assumed between A3 and A4. Thus, though no laser beam was directed to a pad of connection A4, the detection step after charging a pad of A3 will result in a high potential indication from the pads of A4 (indicated by a "1" on the right pad).

In Fig.4B, there are shown four buried connections B1, B2, B3, and B4 between pairs of surface pads. The buried conductors are neither visible nor can they be charged by a laser beam, but they can nevertheless be tested by the method of the invention. The explanations given for Fig.4A with respect to selective charging of pads by laser and subsequent detection of the resulting potentials on pads apply also to the situation of Fig.4B.

In Fig.4C, there are shown several via conductors which interconnect pads located on opposite surfaces of the board. As was mentioned already, these via connections can also well be tested by the method of the invention. The only difference with respect to situations (A) and (B) is that the initial selective charging by a laser beam (L) in method step I is done on one surface of the board, whereas detection of resulting potential distribution (D) by method steps II and III is done on the other surface of the board.

Of course, a circuit board (package substrate) to be tested can have any combination of the electrical connections shown in Fig.4, and there can be more complicated connections (branched conductors, conductor networks, etc.). When the testing is done in suitable sequential steps, each separate "network" can be tested for integrity, and shortcut circuits between "networks" will also be detected easily.

It is of course also possible to test different connecting lines or via connections simultaneously, e.g. if the connections which are tested simultaneously have so much distance from each other that shortcuts between them are not possible.

4) COMPARISON OF SPEEDS FOR E-BEAM TESTING AND FOR LASER TESTING

In E-beam testing technology, there are problems with the separation of high-energy (reflected beam) electrons from low-energy (secondary) electrons if one uses position-sensitive detection. With E-beams, the high-energy electrons of the reflected E-beam (about 1,000 eV) would also reach the channel plates and destroy the voltage contrast information because this information about the voltages is in the low-energy electrons. In photoemission, there are only the electrons emitted with energies in the range 0 eV to 1 eV which also contain the information about the voltages on the surface of the investigated sample.

If the measurement or loading time for a single point is comparable in E-beam and in photoemission technology, the flooding approach which is only useful with laser-excited photoemission leads to a much smaller total measuring time of this latter technique. In testing, one finds that the measuring time for a single spot is four times larger in E-beam technology than with photoemission. For full package testing which allows the flooding approach improvement is therefore much larger.

Claims

1. Method of testing in vacuum the integrity of conducting paths in or on a circuit substrate consisting of non-conducting material, each said conducting path being connected to at least two uncovered pads on any one face of the substrate, characterized by the following steps:

-(a) generating charges in at least one selected pad (P21) on one face of the substrate by a focused laser beam whose energy is sufficient to cause photoelectron emission from each selected pad but insufficient to cause photoelectron emission from said non-conducting substrate material, thus inducing a specific voltage level in each selected pad, and also in each non-selected pad (P22) which is electrically connected to a selected pad;

-(b) causing voltage-dependent photoelectron emission from pads on any one face of the substrate by a flooding laser beam; and

-(c) detecting said voltage-dependent photoelectron emission by evaluating the output of a position-sensitive channel-plate arrangement (15) located in the vicinity of the respective flooded face of the substrate.

2. Method in accordance with claim 1, characterized in that

-steps (a), (b), and (c) are all conducted on the same face of the substrate, for testing the integrity of electrical connections between at least one pair of pads (P21, P22) being both located on the same face of the substrate.

3. Method in accordance with claim 1, characterized in that

-step (a) is conducted on one face (11A) of the substrate, and steps (b) and (c) are conducted on the other face (11B) of the substrate, for testing the integrity of via connections between at least one pair of pads (P31, P32) which are located on different faces of the substrate.

4. Method in accordance with claim 3, characterized in that

-the substrate (11) is turned over by 180 degree between step (a) and step (b), so that a laser device (13) and a channel-plate arrangement (15) of the testing facility can be located all on one side of the substrate location.

5. Method in accordance with claim 3, characterized in that

-the substrate (11) is not moved during the whole testing operation; that the step of directing a focused laser beam to selected pads is executed on one side of the substrate's location; and that the steps of causing and of detecting voltage-dependent photoemission are executed on the other side of the substrate's location.

6. Method in accordance with claim 1, characterized in that

-in an additional step between steps (b) and (c), the electrons emitted by voltage-dependent photoelectron emission from pads are accelerated towards the channel-plate arrangement (15) by providing a respective accelerating voltage (V_{ACC}), and are retarded, after acceleration, by a respective retarding voltage (V_{RET}).

7. Method in accordance with claim 1, characterized in that

-in said detecting step (c), electrons furnished by the position-sensitive channel-plate arrangement (15) are directed to an electroluminiscent layer (17), and that the electroluminiscence pattern excited in said layer (17) is detected by a scanning electronic camera (21).

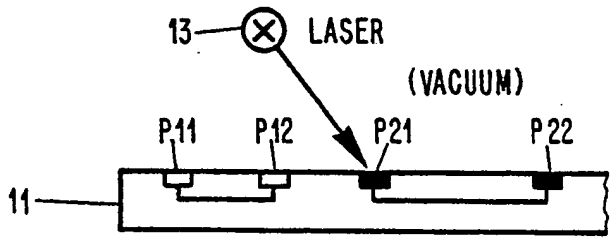
8. Method of testing in vacuum the integrity of conducting via connections in a circuit substrate consisting of non-conducting material, each of said via connections having one pad (P31) on one surface (11A) and another pad (P32) on the other surface (11B) of the substrate, characterized by the following steps:

-(a) generating charges in all pads (P31, P41, P51, P61) on said one surface (11A) of the substrate by a flooding laser beam whose energy is sufficient to cause photoelectron emission from said pads but insufficient to cause photoelectron emission from said non-conducting substrate material, thus inducing a specific voltage level in each pad on said one surface, and also in each pad (P32, P42, P52, P62) on said other surface (11B) which is electrically connected to a pad on said one surface;

-(b) causing voltage-dependent photoelectron emission from pads on said other surface (11B) of the substrate by a flooding laser beam; and

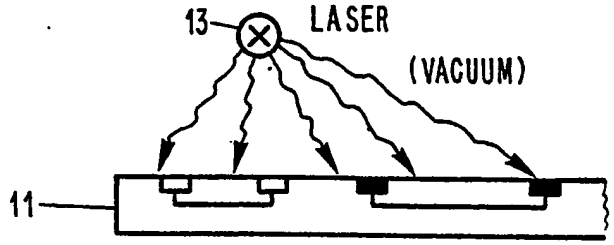
-(c) detecting the pattern of said voltage-dependent photoelectron emission by evaluating the output of a position-sensitive channel-plate arrangement (15') located in the vicinity of said other surface (11B) of the substrate.

FIG. 1 PRINCIPLE



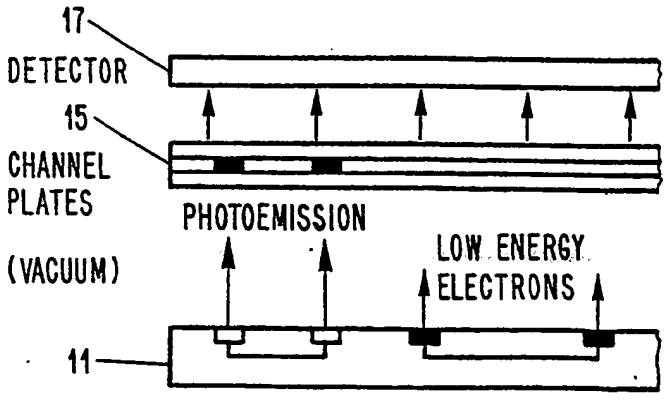
I) CHARGE SELECTIVELY BY SCANNING LASER BEAM

(GENERATING CHARGES BY PHOTO EMISSION)



II) FLOOD BY LASER

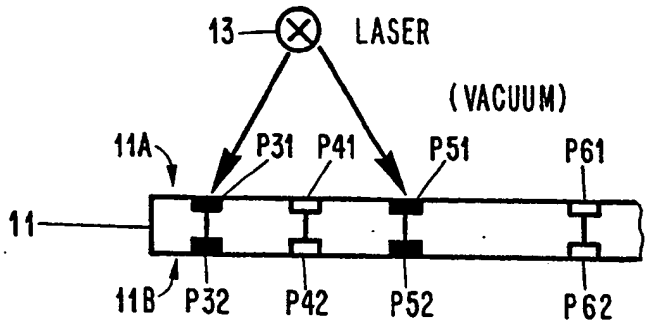
(TO CAUSE PHOTO-EMISSION FROM NON-CHARGED SPOTS)



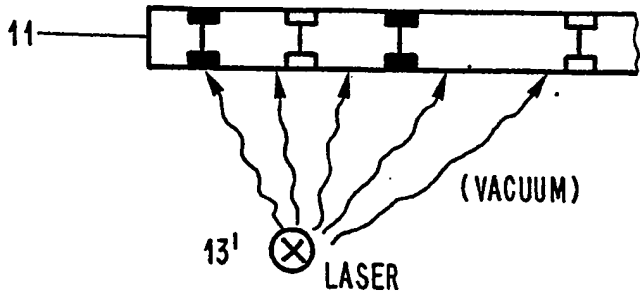
III) DETECT PATTERN OF PHOTOEMISSION

(USING POSITION-SENSITIVE CHANNEL PLATE/-DETECTOR ARRANGEMENT)

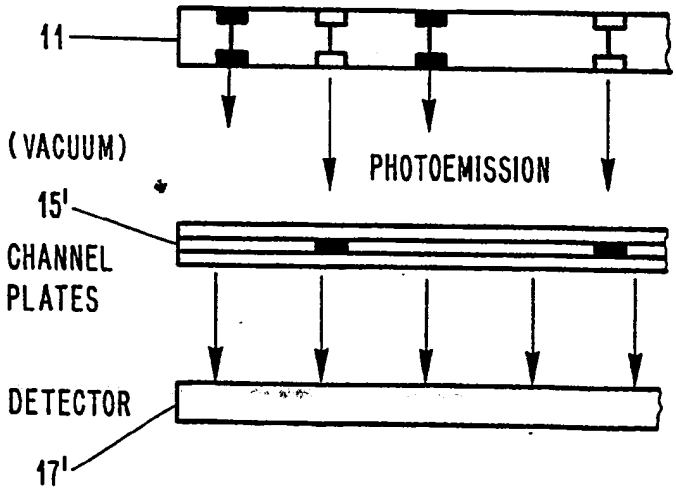
FIG. 2 TESTING VIA CONNECTIONS



I) CHARGE SELECTED PADS ON ONE SIDE BY SCANNING LASER BEAM (FOR SIMULT. TESTING OF ALL VIAS: FLOOD ONE SIDE BY LASER)



II) FLOOD SURFACE ON OTHER SIDE BY LASER



III) DETECT PATTERN OF PHOTOEMISSION ON OTHER SIDE BY CHANNEL PLATE / DETECTOR ARRANGEMENT

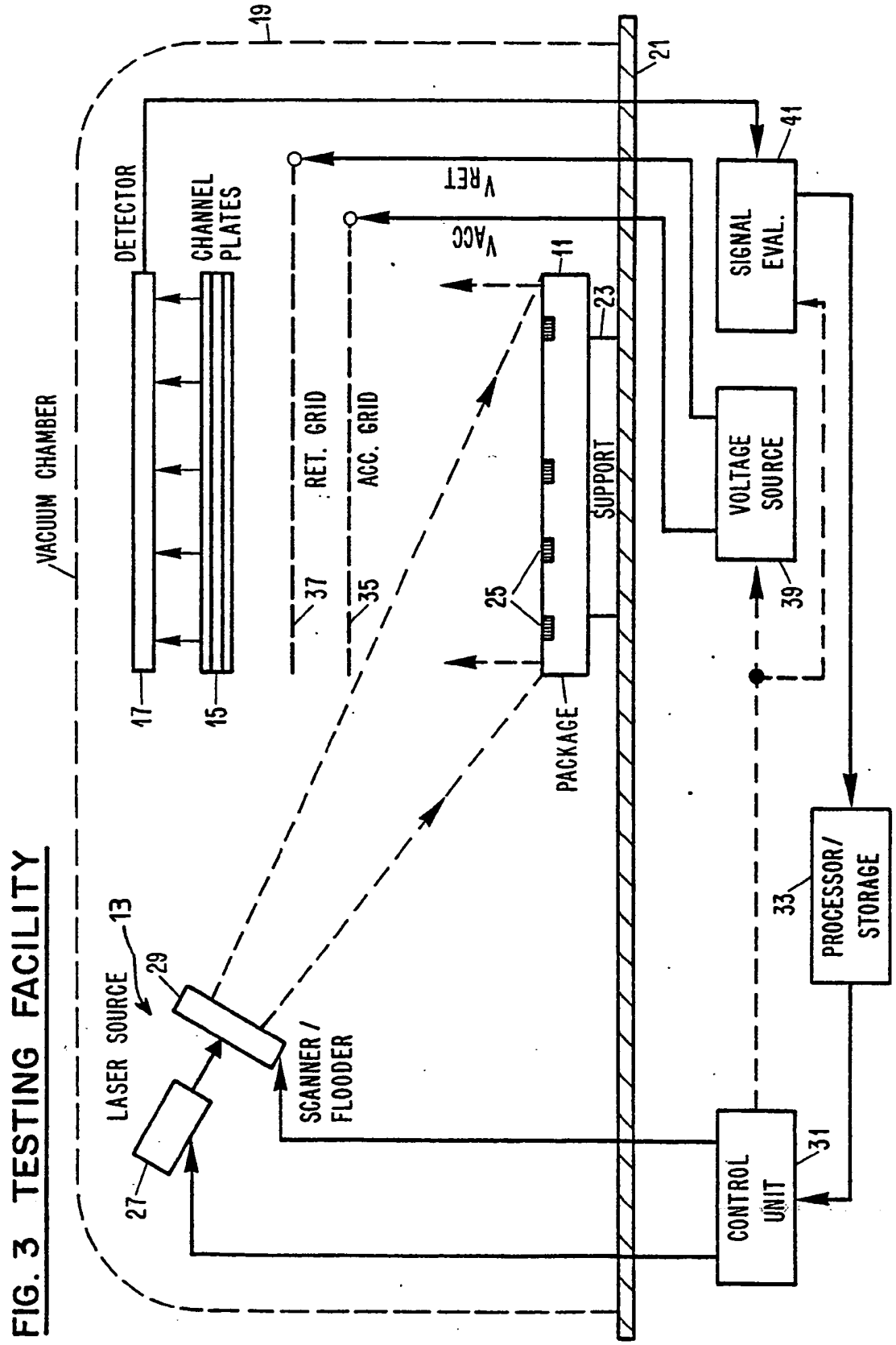
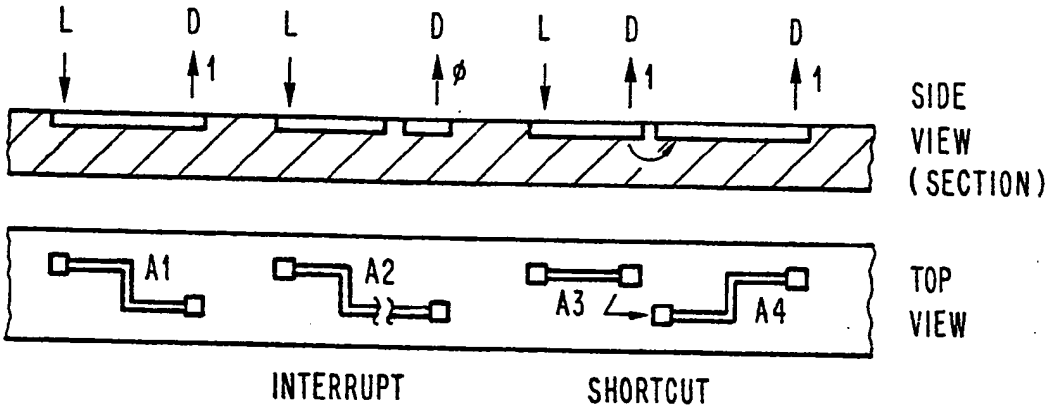


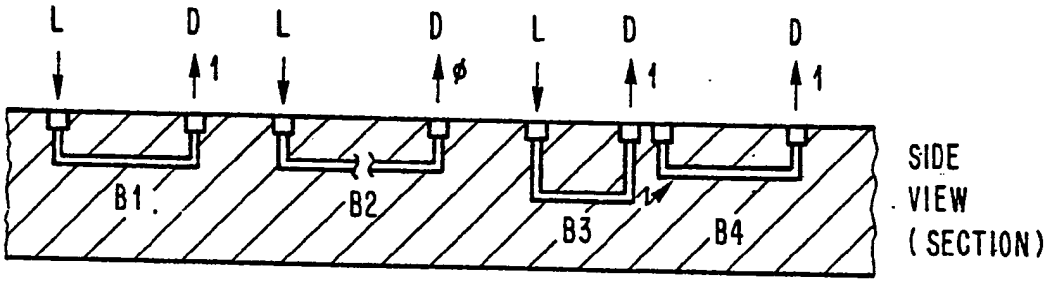
FIG. 3 TESTING FACILITY

FIG.4 TESTING POSSIBILITIES

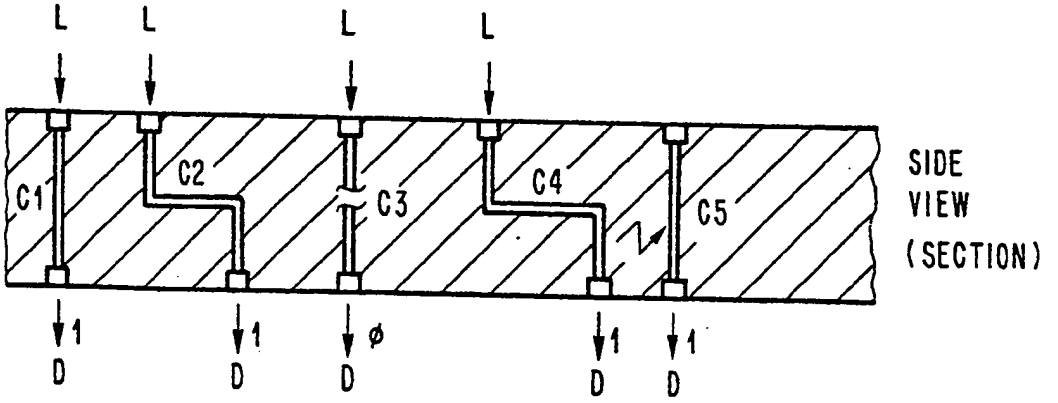
A) SURFACE LINES



B) BURIED LINES



C) VIA CONNECTIONS



L = INITIAL SELECTIVE LASER EXCITATION

D = DETECTION (AFTER FLOODING)

European Patent Office

EUROPEAN SEARCH REPORT

Application number

EP 86 11 4711

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 128 107 (OPTROTECH LTD.) * Page 3, line 28 - page 8, line 8; page 8, lines 26-40; figures 1-3,6 *	1,2	G 01 R 31/28 G 01 R 31/02
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 27, no. 10B, March 1985, pages 5959-5960, New York, US; "Photoelectric test method for PCB conductors" * The whole article *	1,2	
A	EP-A-0 180 780 (IBM) * Column 3, line 11 - column 4, line 10; figure 1 *	1	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 25, no. 3A, August 1982, pages 1171-1172, New York, US; G.W.RUBLOFF: "Contactless measurement of voltage levels using photoemission" * The whole article *		TECHNICAL FIELDS SEARCHED (Int. Cl.4) G 01 R 31/00 H 01 L 21/00 G 01 N 23/00

-/-

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30-06-1987	TRELEVEN C.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO Form 1503 03.82

European Patent Office

EUROPEAN SEARCH REPORT

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	REVIEW SCI. INSTRUMENTS, vol. 49, no. 6, June 1978, pages 756-759, American Institute of Physics, New York, US; M.KUDO et al.: "Computer controlled ESCA for nondestructive surface characterization utilizing a TV-type position sensitive detector" * Page 756, column 2, line 10 - page 757, column 1, line 5; figure 2 *	1,7	
A	NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, vol. 208, no. 1/3, April 1983, pages 373-377, North-Holland Publishing Company, Amsterdam, NL; F.POLACK et al.: "Project of a photoelectron x-ray microscope on ACO storage ring" * Page 374, column 1, line 8 - page 374, column 2, line 30; figure 2 *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
A	US-A-3 436 651 (J.D.HELMS et al.) * Column 2, line 1 - column 3, line 56; figure 1 *	3,5	
A	FR-A-2 380 556 (SECRETAIRE D'ETAT) * Page 6, line 20 - page 7, line 28; figures 1-2 *	6	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30-06-1987	TRELEVEN C.

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, vol. 208, no. 1/3, April 1983, pages 777-784, North-Holland Publishing Company, Amsterdam, NL; D.RIEGER et al.: "A display-type analyzer with an image-processing system for angle-resolved photoelectron spectroscopy" * Page 781, column 2, line 24 - page 782, column 1, line 3; figure 6 *	7	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

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